

Claims:

1. (Currently Amended) A transceiver system comprising:

at least one receiver for receiving one or more signals from one or more transmitters, said one or more received signals having an associated chip rate, said receiver having:

at least one filter for selecting one or more input signals from the received signals;

a sequence extension remover for removing a predetermined number of chips from at least one predetermined position of said received signal to form a modified signal;

a despreader arranged to despread said received signal to a symbol rate and to form a despread signal, said symbol rate being less than said chip rate at which said received signal was spread prior to being received by said receiver, the ratio of the spread rate to the symbol rate being the processing gain of the receiver; and

a frequency domain equalizer ~~for forming~~ arranged to form a frequency equalized signal from said ~~modified-despread~~ despread signal.

2. (Original) A transceiver system according to claim 1, wherein said sequence extension remover has an input for receiving one or more signals output from said at least one filter, and said sequence extension remover has an output coupled to an input of said despreader.

3. (Original) A transceiver system according to claim 1, wherein said despreader has an input for receiving one or more signals output from said at least one filter, and said despreader has an output coupled to an input of said sequence extension remover.

4. (Original) A transceiver system according to claim 2, wherein said despreader has an output, and said frequency domain equalizer has an input, said despreader output being coupled to said input of said frequency domain equalizer.

5. (Original) A transceiver system according to claim 3, wherein said sequence extension remover has an output, and said frequency domain equalizer has an input, said output of said sequence extension remover being coupled to said input of said frequency domain equalizer.

6. (Currently Amended) A transceiver system according to ~~any one of the preceding claims~~1, wherein said at least one receiver further comprises a first converter for converting the modified signal from a serial sequence to a parallel sequence, the first converter having an input coupled to an output of said at least one filter.

7. (Currently Amended) A transceiver system according to ~~any one of the preceding claims~~1, wherein said at least one receiver further comprises a second converter coupled to an output of said frequency domain equalizer for converting the signal output from said frequency domain equalizer from a parallel sequence to a serial sequence.

8. (Original) The transceiver system according to claim 1, wherein said sequence extension remover is arranged to remove a predetermined number of chips carrying data denoting a cyclic prefix and/or a cyclic postfix.

9. (Original) The transceiver system according to claim 1, wherein said at least one receiver further comprises an orthogonal transform block for transforming said signal from a first domain to form a transformed signal in a second domain, said orthogonal transform block having an output coupled to an input of said frequency domain equalizer.

10. (Original) The transceiver system of claim 9, wherein said orthogonal transform block comprises a Fast Fourier Transform block.

11. (Original) The transceiver system of claim 10, wherein said first domain is the time domain and said second domain is the frequency domain.

12. (Original) The transceiver system of claim 1, wherein said at least one receiver comprises an inverse orthogonal transform block for transforming said signal from a second domain to a first domain, said inverse orthogonal transform block having an input coupled to an output of said frequency domain equalizer.

13. (Original) The transceiver system of claim 12, wherein said inverse orthogonal transform block comprises an Inverse Fast Fourier Transform block.

14. (Original) The transceiver system of claim 13, wherein said first domain is the time domain and said second domain is the frequency domain.

15. (Currently Amended) The transceiver system of ~~any one of the preceding claims 1~~, wherein said one or more filters are matched to a pulse shaping network in said transmitter.

16. (Currently Amended) The transceiver system according to ~~any one of claims 12 to 14~~, wherein said at least one receiver further comprises a deinterleaver block having an input coupled to an output of said inverse orthogonal transform block to form a deinterleaved signal to select one or more predetermined signals corresponding to predetermined users.

17. (Original) The transceiver system according to claim 1, wherein said frequency domain equalizer is arranged to equalize a frequency-selective fading channel to a non-frequency selective fading channel.

18. (Currently Amended) The transceiver system according to ~~any one of claims 1, 2, 4 and 6 to 17~~, wherein said at least one transmitter comprises:

at least one spreader for spreading a data packet having one or more blocks to derive a spread sequence for each of said blocks to form a spread signal, said spreader having an input and an output;

a sequence extender for extending each of said blocks using a predetermined number of chips to form an extended spread signal, said sequence extender being coupled to the output of the spreader, said sequence extender having an input and an output; and

a pulse shaper coupled to the output of said sequence extender.

19. (Original) The transceiver system according to claim 18, wherein said at least one transmitter comprises an interleaver for interleaving one or more modulated input signals from one or more users to produce an interleaved signal, said interleaver having an output coupled to an input of said at least one spreader.

20. (Original) The transceiver system according to claim 19, wherein said at least one transmitter further comprises a first converter for converting the interleaved signal from a serial sequence to a parallel sequence, the first converter having an output coupled to the input of said at least one spreader and an input connected to said output of said interleaver.

21. (Currently Amended) The transceiver system according to ~~any one of claims 18 to 20~~, wherein said at least one transmitter further comprises a second converter coupled between said spreader and said sequence extender for converting said spread signal from a parallel sequence to a serial sequence.

22. (Currently Amended) A transceiver system according to ~~any one of claims 1, 3, and 5 to 17~~, wherein said at least one transmitter comprises:

a sequence extender for extending each of a number of blocks in an incoming signal using a predetermined number of chips to form an extended signal, said sequence extender having an output and an input, said incoming signal comprising at least one data packet;

at least one spreader for spreading said extended signal to derive a spread sequence for each of said blocks to form a spread signal, said spreader having an input and an output, said input of said spreader being coupled to said output of said sequence extender; and

a pulse shaper coupled to the output of said spreader to provide a transmitter output signal.

23. (Original) A transceiver system according to claim 22, wherein said at least one transmitter further comprises a first converter for converting the incoming signal from

a serial sequence to a parallel sequence, the first converter having an output coupled to the input of said sequence extender.

24. (Original) A transceiver system according to claim 23, wherein said at least one transmitter further comprises an interleaver for receiving one or more modulated input signals from one or more users, said interleaver having an output coupled to an input of said first converter.

25. (Currently Amended) A transceiver system according to ~~any one of claims 22 to 24~~, wherein said at least one transmitter further comprises a second converter having an input coupled to the output of said spreader for converting the signal output from said spreader from a parallel sequence to a serial sequence, the second converter having an output coupled to an input of said pulse shaper.

26. (Currently Amended) A transceiver system according to ~~any one of claims 22 to 24~~, wherein said pulse shaper matches the filter of said at least one receiver.

27. (Original) A method for transmitting signals, said method comprising the steps of:
spreading, by at least one spreader, a data packet having one or more blocks to derive a spread sequence for each of said blocks and to form a spread signal;

extending, by a sequence extender, each of said blocks in said spread signal using a predetermined number of chips to form an extended spread signal, said spread signal being received from a spreader output of said at least one spreader; and

shaping, by a pulse shaper coupled to an output of said sequence extender, said extended spread signal; and interleaving, in at least one interleaver, one or more modulated input signals from one or more users to form an interleaved signal, before the spreading step

28. (Cancelled)

29. (Currently Amended) The method of claim ~~28~~27, further comprising converting, in a first converter, the interleaved signal from a serial sequence to a parallel sequence, before the spreading step.

30. (Currently Amended) The method of ~~any one of claims 27 to 29~~, further comprising converting said spread signal from a parallel sequence to a serial sequence before the extending step.

31. (Original) A method for transmitting signals, said method comprising the steps of:
extending, by a sequence extender, each of a number of blocks in an incoming signal using a predetermined number of chips to form an extended signal, said incoming signal comprising at least one data packet;

spreading, in at least one spreader, said extended signal received from an output of said sequence extender to derive a spread sequence for each of said blocks to form a spread signal; and

shaping, in a pulse shaper, said spread signal received from an output of said at least one spreader to provide a transmitter output signal.

32. (Original) The method of claim 31, further comprising the step of converting the incoming signal from a serial sequence to a parallel sequence before the extending step.

33. (Currently Amended) The method of ~~any one of claims 31 and 32~~, further comprising interleaving, in at least one interleaver, said one or more modulated input signals from one or more users to form an interleaved signal, prior to the extending step.

34. (Currently Amended) The method of ~~any one of claims 31 to 33~~, further comprising converting said spread signal, received from said spreader, from a parallel sequence to a serial sequence, prior to the pulse shaping step.

35. (Currently Amended) The method of ~~any one of claims 31 to 34~~, further comprising shaping said signal using a pulse shaper which matches a input filter of at least one receiver.

36. (Currently Amended) A method for processing a received signal comprising the steps of:

receiving one or more signals from one or more transmitters, said one or more received signals having an associated chip rate;

selecting, using at least one filter, one or more input signals from the received signals;

removing, in at least one sequence extension remover, a predetermined number of chips from at least one predetermined position of said received signal to form a modified signal;

despreading, in at least one despreader, said received signal to a symbol rate and to form a despread signal, said symbol rate being less than said chip rate at which said received signal was spread prior to being received by said receiver, the ratio of the spread rate to the symbol rate being the processing gain of the receiver; and

forming, in at least one frequency domain equalizer, a frequency equalized signal from said ~~modified~~ despread signal.

37. (Original) A method according to claim 36, wherein said step of removing said sequence extension is before said despreading step and after said selecting step.

38. (Original) A method according to claim 36, wherein said despreading step is before said step of removing said sequence extension and after said selecting step.

39. (Original) A method according to claim 38, wherein the step of removing said sequence extension is before said step of forming, in at least one frequency domain equalizer, a frequency equalized signal and after said despreading step.

40. (Original) A method according to claim 37, wherein the despreading step is before the step of forming the frequency equalized signal.

41. (Currently Amended) A method according to ~~any one of claims 36 to 40~~, further comprising converting the modified signal from a serial sequence to a parallel sequence after the selecting step.

42. (Currently Amended) A method according to ~~any one of claims 36 to 41~~, further comprising converting the frequency equalized signal from a parallel sequence to a serial sequence.

43. (Original) The method of claim 36, wherein the step of removing said sequence extension comprises removing a predetermined number of chips carrying data denoting a cyclic prefix and/or a cyclic postfix.

44. (Original) The method of claim 36, further comprising transforming in an orthogonal transform block said signal from a first domain to form a transformed signal in a second domain, before the step of forming said frequency equalized signal.

45. (Original) The method of claim 44, wherein said transforming step comprises applying a Fast Fourier Transform process to said signal.

46. (Currently Amended) The method of ~~any one of claims 44 or 45~~, wherein said transforming step comprises transforming said signal from the time domain to the frequency domain.

47. (Original) The method of claim 36, further comprising applying, after the step of forming a frequency equalized signal, applying an inverse orthogonal transformation to said signal for transforming said signal from a second domain to a first domain.

48. (Original) The method of claim 47, wherein the step of applying an inverse orthogonal transformation comprises applying an Inverse Fast Fourier Transform process.

49. (Currently Amended) The method of ~~any one of claims 47 or 48~~, wherein the step of applying an inverse orthogonal transformation comprises transforming the signal from the time domain to the frequency domain.

50. (Currently Amended) The method of ~~any one of claims 36 to 49~~, further comprising matching said at least one filter to a pulse shaping network in a transmitter.

51. (Currently Amended) The method of ~~any one of claims 47 to 49~~, further comprising deinterleaving said inverse orthogonally transformed signal to select one or more predetermined signals corresponding to predetermined users to form a deinterleaved signal.

52. (Original) The method of claim 36, wherein the step of forming a frequency equalized signal comprises equalizing a frequency-selective fading channel to a non-frequency selective fading channel.

53. (Currently Amended) A code division multiple access (CDMA) system comprising at least one transceiver system according to ~~any one of claims 1 to 26~~.

54. (Currently Amended) An ultrawide band (UWB) system comprising at least one transceiver system according to ~~any one of claims 1 to 26~~.